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L3	L2 same (compar$3 near10 monitor$3)	31	L3
L2	generat$3 same trigger same output same condition	10926	L2
L1	generat$3 near5 (trigger adj1 output) near5 (trigger adj1 condition)	5	L1

END OF SEARCH HISTORY

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L4	L3	0	L4
DB=USPT,USOC; PLUR=YES; OP=OR			
L3	L2 same (compar$3 near10 monitor$3)	31	L3
L2	generat$3 same trigger same output same condition	10926	L2
L1	generat$3 near5 (trigger adj1 output) near5 (trigger adj1 condition)	5	L1

END OF SEARCH HISTORY

Refine Search

Search Results -

Terms	Documents
L5 and (compar$3 near10 monitor$3)	8

Database:
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Search: L6

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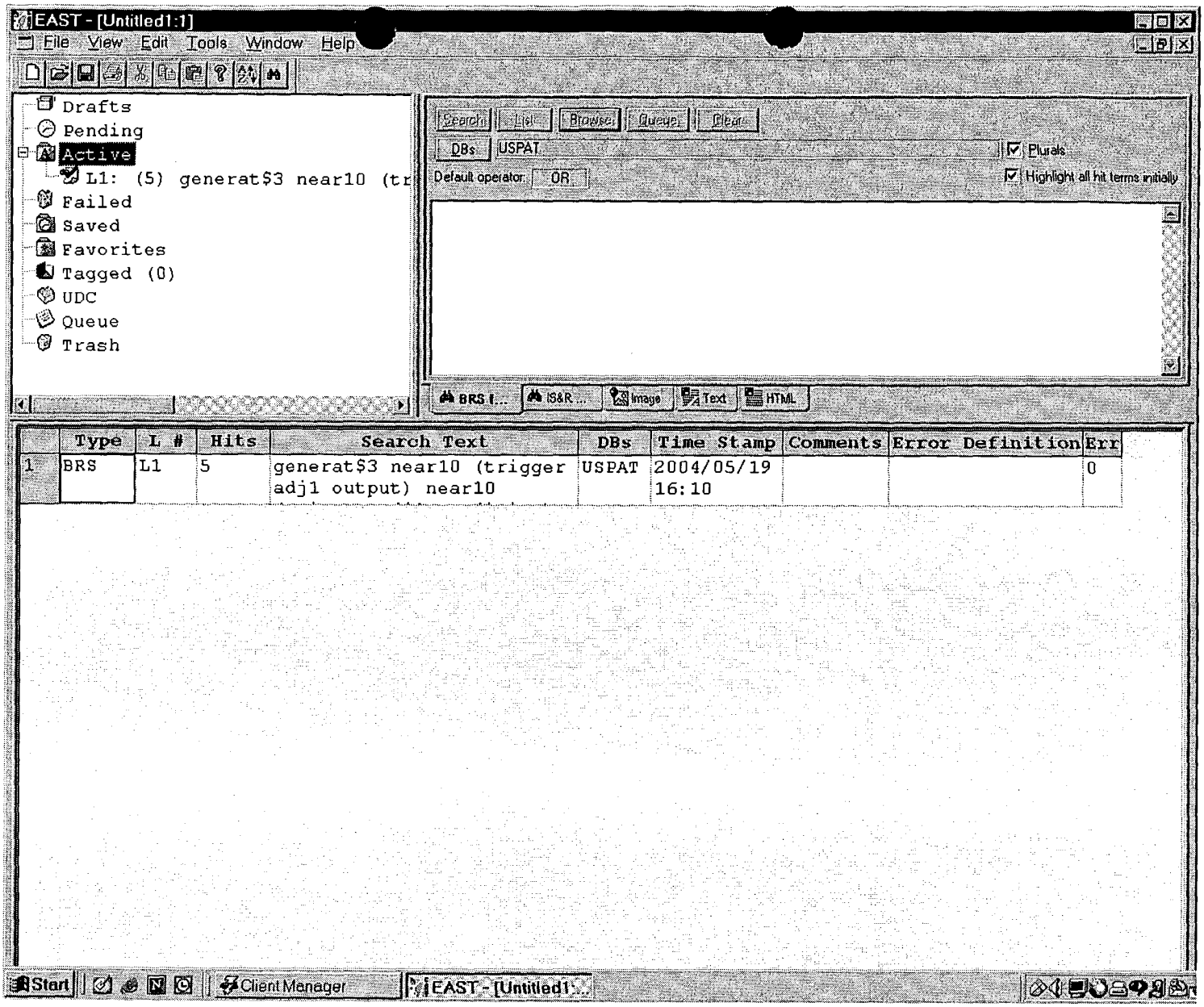
DB=USPT,USOC; PLUR=YES; OP=OR			
L6	L5 and (compar$3 near10 monitor$3)	8	L6
L5	L2.ab.	83	L5
DB=EPAB,JPAB,DWPI,TDBD; PLUR=YES; OP=OR			
L4	L3	0	L4
DB=USPT,USOC; PLUR=YES; OP=OR			
L3	L2 same (compar$3 near10 monitor$3)	31	L3
L2	generat$3 same trigger same output same condition	10926	L2
L1	generat$3 near5 (trigger adj1 output) near5 (trigger adj1 condition)	5	L1

END OF SEARCH HISTORY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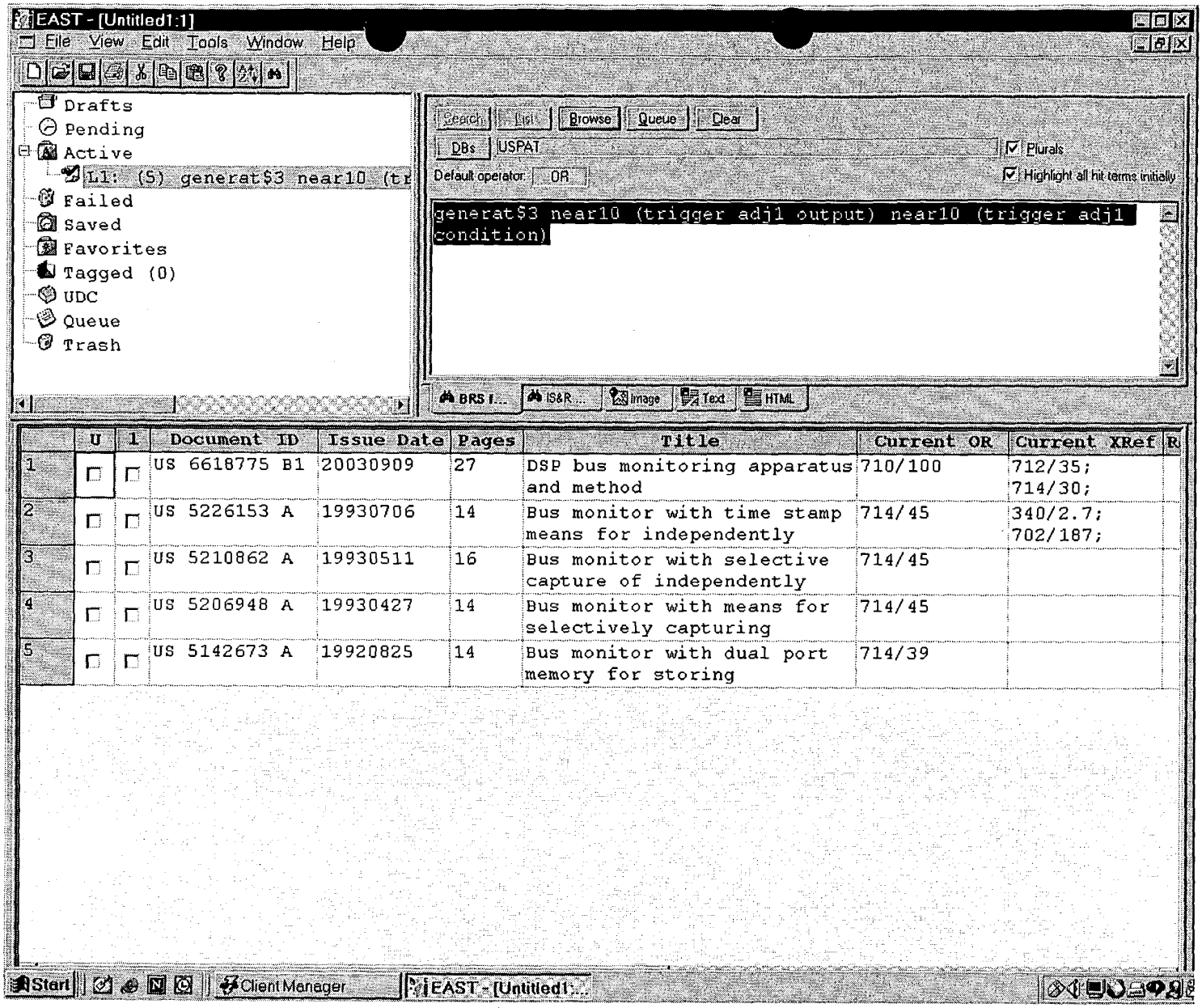
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U 1 Document ID Issue Date Pages Title Current OR Current XRef R
1 US 6618775 B1 20030909 27 DSP bus monitoring apparatus and method 710/100 712/35; 714/30;
2 US 5226153 A 19930706 14 Bus monitor with time stamp means for independently 714/45 340/2.7; 702/187;
3 US 5210862 A 19930511 16 Bus monitor with selective capture of independently 714/45
4 US 5206948 A 19930427 14 Bus monitor with means for selectively capturing 714/45
5 US 5142673 A 19920825 14 Bus monitor with dual port memory for storing 714/39
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1 **Compact 12.5 MW, 55 kV solid state modulator**
Richardson, R.; Rush, R.J.; Iskander, S.M.; Gooch, P.;
Pulsed Power Plasma Science, 2001. IEEE Conference Record - Abstracts , 17 June 2001
Pages:583

[Abstract] [PDF Full-Text (50 KB)] IEEE CNF

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2 **Pulse shortening causes in high power BWO and TWT microwave so**
Goebel, D.M.;
Plasma Science, IEEE Transactions on , Volume: 26 , Issue: 3 , June 1998
Pages:263 - 274

[Abstract] [PDF Full-Text (492 KB)] IEEE JNL

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3 **Experimental studies on performance of a nonequilibrium disk MHD generator with radio-frequency preionization**
Fujino, T.; Murakami, T.; Okuno, Y.; Yamasaki, H.;
Plasma Science, IEEE Transactions on , Volume: 31 , Issue: 1 , Feb. 2003
Pages:166 - 173

[Abstract] [PDF Full-Text (788 KB)] IEEE JNL

---

4 **High-power microwave generation using a ferroelectric cathode ele gun**
Hayashi, Y.; Song, X.; Ivers, J.D.; Flechtner, D.D.; Nation, J.A.; Schacter, L.;
Plasma Science, IEEE Transactions on , Volume: 29 , Issue: 4 , Aug. 2001
Pages:599 - 603

[Abstract] [PDF Full-Text (92 KB)] IEEE JNL

5 **A 100 kV, 1 kHz triggered pulse generator**
MacGregor, S.J.; Turnbull, S.M.; Tuema, F.A.; Farish, O.;
Power Modulator Symposium, 1996., Twenty-Second International , 25-27 Ju
1996
Pages:153 - 156

[Abstract] [PDF Full-Text (352 KB)] **IEEE CNF**

6 **An energy balance simulation tool for TOMS-EP**
Mackowski, M.J.; Martin, D.K.;
Energy Conversion Engineering Conference, 1996. IECEC 96. Proceedings of t
31st Intersociety , Volume: 1 , 11-16 Aug. 1996
Pages:641 - 646 vol.1

[Abstract] [PDF Full-Text (500 KB)] **IEEE CNF**

7 **Unstable behavior of parallel fuses as an opening switch**
Shimomura, N.; Nagata, M.; Grabowski, C.; Akiyama, H.;
Pulsed Power Conference, 1995. Digest of Technical Papers. Tenth IEEE
International , Volume: 2 , 3-6 July 1995
Pages:1109 - 1114 vol.2

[Abstract] [PDF Full-Text (540 KB)] **IEEE CNF**

8 **High density compact tunable PFN-Marx modulators**
Phelps, D.A.;
Power Modulator Symposium, 1990., IEEE Conference Record of the 1990
Nineteenth , 26-28 June 1990
Pages:507 - 510

[Abstract] [PDF Full-Text (560 KB)] **IEEE CNF**

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A 100 kV, 1 kHz triggered pulse generator

MacGregor, S.J. Turnbull, S.M. Tuema, F.A. Farish, O.
Strathclyde Univ., Glasgow, UK;

This paper appears in: **Power Modulator Symposium, 1996., Twenty-Second International**

Meeting Date: 06/25/1996 - 06/27/1996
Publication Date: 25-27 June 1996
Location: Boca Raton, FL USA
On page(s): 153 - 156
Reference Cited: 8
Number of Pages: vi+260
Inspec Accession Number: 5558178

Abstract:
The performance of a repetitive pulse **generator** system is described. The **generator** is capable of operation under **triggered**, untriggered and single shot **conditions**. When operated in a **triggered** mode, the **generator** produces **output** voltages of up to 100 kV, at a pulse repetition frequency (PRF) which is fully controllable over the range 1 Hz to 1.2 kHz. In an untriggered mode, the PRF can be increased to 5 kHz

Index Terms:

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power supplies to apparatus pulse **generators** pulsed power technology **trigger** circuits 1 Hz to 1.2 kHz 1 kHz 100 kV 5 kHz performance pulse repetition frequency pulsed power **generators** repetitive pulse **generator** system single shot **conditions** **triggered conditions** **triggered** pulse **generator** untriggered **conditions**

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Compact 12.5 MW, 55 kV solid state modulator

Richardson, R. Rush, R.J. Iskander, S.M. Gooch, P.

This paper appears in: **Pulsed Power Plasma Science, 2001. IEEE Conference Record - Abstracts**

Meeting Date: 06/17/2001 - 06/22/2001
Publication Date: 17-22 June 2001
Location: Las Vegas, NV USA
On page(s): 583
Number of Pages: 624
Inspec Accession Number: 7176064

Abstract:
Summary form only given, as follows. The paper will describe a modulator system developed by the Marconi Applied Technologies High Voltage Engineering Group for driving high peak power magnetrons and klystrons. The modulator unit is a compact (0.1 M3 and 91 Kgs), fully integrated system, with an **output** capability of 55 kV at 250 A. Pulse widths in the range 0.5 uS to 6 uS at duties of up to 0.1%. The modulator switch is of the direct or active switched type, using a series/parallel bank of Mosfets, arranged into 75 modules, to partially discharge an integral capacitor bank into the load. The duty cycle at the **output** is an amplified representation of the low level drive waveform

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applied to the **trigger** input and is not limited to a regular pulse train. The modulator system includes a microprocessor based control system, incorporating all support LT and heater supplies, a specially developed capacitor charge power supply incorporating a close loop control system regulating on peak current and the high voltage switch unit. Thus providing an end user philosophy of "Three-phase mains power & **trigger** input for a microwave tube drive **output**". The modulator is cooled by, simple forced oil system with an integral oil/water heat exchanger. The paper will discuss the overall design philosophy, the methods of realizing key components, such as **trigger generation**/steering and the floating drives to modules. Fault detection and monitoring will be discussed for fault working during load arc/load short circuit **conditions**. CAD and FE tools used during the development and some of the results from system/life test programs will be discussed. Future expansion plans and adaptation of the system will be outlined, including the use of alternative switch devices (such as IGBT's) and operation with none uniform high duty cycle burst waveforms

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Index Terms:

klystrons magnetrons pulsed power supplies 12.5 MW 250 A 55 kV Mosfets capacitor charge power supply close loop control system end user philosophy fault working floating drives forced oil system fully integrated system high duty cycle burst waveforms high voltage switch unit integral capacitor bank integral oil/water heat exchanger klystrons level drive waveform load arc/load short circuit **conditions** magnetrons microprocessor based control system microwave tube drive **output** modulator switch modulator system modulator unit pulse widths regular pulse train series/parallel bank solid state modulator switch devices **trigger generation**/steering

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L3: Entry 9 of 31 File: USPT Jul 6, 1993

DOCUMENT-IDENTIFIER: US 5226153 A
TITLE: Bus monitor with time stamp means for independently capturing and correlating events

Detailed Description Text (29):
The primary elements comprising Trigger Control 38 are shown in the lower right portion of FIG. 2 and include Trigger Enable Register (TRIGENR) 90, Trigger Memory (TRIGMEM) 92, Illegal/Error Condition Detector (ILGL/ER) 94, Trigger Detector Logic (TRIGDET) 96, Trigger Registers (TRIGREG) 98 and Time Stamp Counter (TSC) 100. As will be described below, the outputs from TRIGMEM 92, ELGL/ER 94 and the inputs from EXTTRG 42 are trigger signals representing the occurrence of conditions being monitored while TRIGENR 90 stores information, in the form of trigger enabling codes, determining what particular monitored conditions will result in a sampling trigger while. TRIGDET 96 and TRIGREG 98 compare the triggers representing the occurrence of conditions being monitored with the present and previous trigger condition inputs from TRIGENR 90 and generate a trigger output, TRIGS, when a set of monitored conditions match the criteria stored in TRIGENR 90.

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L3: Entry 9 of 31 File: USPT Jul 6, 1993

US-PAT-NO: 5226153
DOCUMENT-IDENTIFIER: US 5226153 A

TITLE: Bus monitor with time stamp means for independently capturing and correlating events

DATE-ISSUED: July 6, 1993

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
DeAngelis; Douglas J.	Woburn	MA		
Maddox; Henry W. J.	Franklin	MA		
Peters; Arthur	Sudbury	MA		
Rathbun; Donald J.	Methuen	MA		

ASSIGNEE-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY	TYPE CODE
Bull HN Information Systems Inc.	Billerica	MA			02

APPL-NO: 07/ 944793 [PALM]
DATE FILED: September 14, 1992

PARENT-CASE:
This is a continuation of copending application Ser. No. 07/455,668, filed on Dec. 22, 1989, now abandoned.

INT-CL: [05] G06F 11/30, G06F 11/34

US-CL-ISSUED: 395/575; 364/550, 364/DIG.1, 364/264, 364/921.8, 364/949.3, 364/242.4, 340/825.06
US-CL-CURRENT: 714/45; 340/2.7, 702/187, 714/27

FIELD-OF-SEARCH: 395/575, 371/29.1, 371/68.3, 364/550, 340/825.06

PRIOR-ART-DISCLOSED:

U.S. PATENT DOCUMENTS

Search Selected Search ALL Clear

	PAT-NO	ISSUE-DATE	PATENTEE-NAME	US-CL
☐	3748650	July 1973	Garcia et al.	395/275
☐	3818458	June 1974	Deese	364/200

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☐	3906454	September 1975	Martin	364/200
☐	4166290	August 1979	Furtman et al.	364/900
☐	4367525	January 1983	Brown et al.	364/200
☐	4477873	October 1984	Mc Carley	364/200
☐	4521849	June 1985	Wilder, Jr.	364/200
☐	4628511	December 1986	Stitzlein et al.	364/900
☐	4764863	August 1988	Silverthorn, III et al.	395/575
☐	4949252	August 1990	Hauge	364/200
☐	4996703	February 1991	Gray	379/40
☐	5027297	June 1991	Garitty et al.	364/569
☐	5142673	August 1992	De Angelis et al.	395/575

ART-UNIT: 236

PRIMARY-EXAMINER: Chan; Eddie P.

ATTY-AGENT-FIRM: Clapp; Gary D. Solakian; John S.

ABSTRACT:

A monitor for selectively detecting and recording conditions at selected points within a system during operation includes trigger logic connected from first selected points and responsive to selected conditions occurring at each of the first points for generating corresponding trigger outputs representing the occurrence of the selected conditions and a silo bank memory having a sub-silo for each second point. Each sub-silo has a first sub-silo segment with data inputs connected from the corresponding second point for recording data from the second point and a second sub-silo segment with data inputs connected from a time stamp generator. Silo write control logic is responsive to the trigger outputs to write the data representing the conditions present at each second point and the time stamp output of the time stamp generator into the corresponding sub-silo segments of the silo bank upon occurrence of a corresponding trigger output so that each condition recorded in the silo bank memory as the result of a trigger output has associated with it the time stamp count representing the relative time of occurrence of the trigger output.

11 Claims, 4 Drawing figures

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L3: Entry 27 of 31 File: USOC Aug 24, 1965

DOCUMENT-IDENTIFIER: US 3202804 A
TITLE: Method and apparatus for monitoring the operation of a system

OCR Scanned Text (20):
21 of a boundary@ pu@ye; yoltaize level detecting means co nected to said fir.st and second means for comparing each @.of said first voltaae signals wit'i at least on@- limit signal and generatin- at least one output signal in response to 'the value of said first signal reaching its respective limit signal value; and means including AND and OR circuits conne,cted to said third-named means for comparing@presele@ted groups of @aid.output signals for determining where @aid] @oiiii defined by said variable input signals is located with respect to seiid ciirve. S. A computer system compri@ing d plurality of varlable inj@ut - signals defining an operating condition; first inean@ responsive to' said input signals for gener ng a plurality of variable first signals defining an opeiating point, said first means including ir. ans for gencratin.one signal representing the sum of a portion of said input variables and means for generating another signal representing the ratio between said one @ signal and at least one of said input signals-, second means for generating a plurality of limit signals, at least one of said limit signals for each first signal, said plurality of limit signals defining an operating curve b6und-,Lry; third means, including a plurality of voltage level detecting means, @ connected to said first and second means for comparing each of said first signals with at least one limit signal and generating a second signal when said first signal is less than said limit value and a third signal in response to the value of said first signal reaching its respective limit value; and fourth means for comparing preselected groups of said second and third signals and generating an indicating signal, said indicating signal having a first value when all of said input signals have failed to reach said limit values and a second value when at least one preselected input signal has reached said operating curve boundary, and means responsive to said indicating signal for controlling at least one of said variable input signals. 6. A monitoring system compri@ing first means respons.ve to a plurality of input signals from a system to be monitored for providing a plurality of first signals representing pertinent parameters of said system and defining an operating condition of said system, second means for generating a plurality of sets of limit value signals, each of said sets defining a boundary curve, said plurality of boundary curves defining a plurality of areas of operation, third means responsive to said first means for comparing each of said first signals with one limit value signal in each of said plurality of sets of limit values and generating a third signal when said limit value has been exceeded and a fourth signal when said first signal is less than said li-init value, logic means responsive to @said third nicans for comparing said third and fourth si.-nals in preselected grolips and generating at least one signal representing the location of said operat,ng condition with respect to at least one of said boundary curves, and means f6r indicating the relative location of said operating condition with respect to at least one of said curves. 7. A monitoring system comprising first means providing a plurality of parameter signals representing values of pertinent parameters of a system to be mon' 1- tored and deflning an operating condition of said monitored system, second means for generating a pluraiity of signals representing a first set of limit values, said first limit values defining a first operating curve, third means for generating a plurality of signals representing a second set of limiting values, said second limit values defining a second operating

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curve, fourth means connected to said first and second means for comparing each of said parameter signals with one of the limit values of said first set and generating first output signals indicating when said parameter signals have reached and have failed to reach said limit values of said first set, fifth means connected to said first and third means for comparing each of said parameter signals with one of the limit values of said second set and generating second output signals 22, indicating when said parameter sianals @have re ached and have failed- to. reach said limit values of said second set, sixth@ means@ responsive to said first output signals for generating an indicating signal 4efining the relative location of said operating condition with respect to said first o e at' p r mg curve, sevent h means resi)onsive to said fifth n@ea4s for generat,iiig] an indicating signal defining the relative @locatidn of s@id overating curve, and means responsive to said ind.icating signqls of said sixth and 10 seventh means for indicating the relative location of said operatm.- co.ndition with respect to both said first and second operating curves. 8. A m6nitoring system comprising first means for providing . a plurality of first signals r,-presen ting the 15 values 6f pertinent parameters of a system to be moni- ' tored; second means -respotisive to said first ineans comparing each of said first signals with at least one preselected limit 'value for generating a plurality of second and third signalsi each of said second'signals being gen- 20 erated when an associated first signal is within said limit value, each of said third signals being gen@-rated when an associated first signal has reached said lirnit value; third means comparing preselected groups of said second and third signals for generating a plurality of fourth and 25 fifth signals' each of said fourth signals being generated when a @preselected group has a predetermined relation- ship, each of said fifth signals being generated when a preselected group has another predetermined relationship; and fourth ii@eans responsive to preselected groups of 30 said fourth and fifth signals for indicating whether or not said monitored system is operating within acceptable boundary conditions, said boundary conditions being defined by said preselected limit values. 9. The monitoring system of claim 8 wherein said 35 third means includes a plurality of OR circuits connected to said second means and responsive to preselected groups of said second and third signals for comparing said si.-nals. 10. The monitoring system of claim 8 wherein said 40 fourth means includes at least one AND circuit responsive to said fourth and fifth signals for comparing preselected groups of said fourth and fifth signals and generating an indicating signal when said group has a predetermined relationship. 45 ill. A monitoring system comprising a plurality of pertinent parameter signals representing the operating condition of a system to be monitored; first means responsive to said parameter signals for generating first voltage signals representing an operating point, 50 means including at least one means for co g at least two of said parameter signals in a predetermined relation and generating a first voltage signal representing said relation; second means for comparing each of said first signals Avith at least one preselected limit value an 55 for generating a plurality of second and third signals, each of said second signals being generated when an associated first signal is within said limit value, each of said third signals being generated when an associated first signal has reached said Emit value,- logic means com- selected groups of said second and third signals 60 paring pre for generating a plurality of fourth and fifth signals, each of said fourth signals being generated when a preselected group has a predeterniined- relationship, each of said fifth signals bein.- generated when a preselected 65 group@ has another relationship-, and fourth means responsive to preselected groups of said fourth and fifth signals for indicating whether or not said monitored system is operating within the boundary conditions defined by said preselected limit values. 70 12. A computer comprising a plurality of first means for generating a plurality of variable first voltage signals representing pertinent parameters defining a point; a pluraety of trigger means each including a voltage level detecting means, each t-rigger means being responsive to 75 one of said first signals for comparing said first signal

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L3: Entry 30 of 31 File: USOC Apr 8, 1958

DOCUMENT-IDENTIFIER: US 2830120 A
TITLE: Electronic switching system

OCR Scanned Text (70):
45 stage responds by sending a negative signal through the "or" gate to the "inhibitor" gate. This allowi the continuing transmission of register drivo pulses -to the ring pulser circuit, and the allottdr continues its stepping process until it finds an idle finder. If desired, a line finder may be taken out of service for repairs by placing a negative potential on its allotter start lead AS. The allofter will theh skip over this particular link, thinking it is busy, and will allot a succeeding idle link. Turning our attention now to the emergency pulse generator circuit of the allotter, it will b,e remembered that the allotter normally operates to allot a new link in response to the allotter start signal received fr6m the allotted line finder. In the, ev&ht of failure of the line finder to seize the calling line, no allotter S-tart signal would be received, and the allotter would remain permanently, locked to the faulty link. To prevent this, a monitor circuit is incorporated withili the allotter which examines the multiplexer pulses on conductor MPX, and compares them with the fmder busy pulses on conductor FB. 'In normal operation of the system, every multiplexer pulse wiH have a companion busy pulse, originating either in a line finder or a connector. The inonitor cir6uit comprises an "inhibitor" gate which is arranged so that afl unguarded multiplex.er pulses are transmitted. If' more than a reasonable number of unguarded multi-' plexer pulses are passed, allowing ample finding time, for the allotted line finder, then the emergency pulse generator is brought into play to generate a single emergency pulse. This pulse is passed through the second "or" gate described previously and serves to operate the ring driver transistor 1226, which in tum, steps the allotter to the next link. Diodes CD1212 and CD1213 comprise the "inhibitor" gate. Conductor MPX and conductor FB connect to the anode ternu'nals of CD1212 and CD1213, respectively. It will be remembered that conductor MPX stands at ground potential except when a negative pulse is connected thereto and conductor FB stands at -7.5 volts except when a positive pulse is connected thereto. Tbus, in the absence of pulses, diode CD1212 conducts so that the gate output is at ground potential and diode CD1213 is cut off. If an uigilarded multiplexer pulse is received, that is, conductor MPX goes negative and condutcor FB remains negative, a negative output is realized from the gate. If the multiplexer pulse has a companion pulse, that is, conductor MPX goes negative and conductor FB rises to approximately ground- potential, diode CD1213, conducts and diode CD1212 is cut off so that the output of the gate remains at ground potential. Thus, negative pulses, which correspond to unguarded multiplexer.pulses, are coupled through capacitor C1204 to, the base circuit of- transistor 1230. Transistor 1230 is connected as a monostable oscillator and its operation is similar to previously described monostable oscillators. Briefly' transistor 1230 is biased for non- conduction by virtue of base bias from ground through resistor R1207, and emitter bias from -7.5 volts throtigh resistor R1209. The negative impulse co-.inected to the base circuit serves to trigger the oscillator into the saturation region. The pulse is terminated when capacitor C1205, which is connected between the e-tnitter and base, becomes charged from -16.5 volts through resistor R1209, the collector, base, and emitter of transistor 1230. When transistor 1230 is rendered non-conductive, capacitor C1205 discharges through ihe back emitter resistance. A positive going output pulse is taken from across corector load resistor R1209 and coupled through

capacitor C1206 to the base circuit of transistor 1240. The positive peak of the pulse, which has a swing of approximately 9 volts, is clamped to +7.5 volts by diode CD1214 which, of course, conducts when its anode potential excceds +7.5 volts. The negative swing which occurs at the termination of the pulse serves to cut off diode CD1214 and tO 46 render transistor 1240 conductive. The time constant of the RC ndtwork, compiising capacitok C1206 and resistor R1210, is sufficie-ntly long so that trahsistor 1240 conducts for an entire frame of 1000 microseconds. Up6n application of succeeding pulses, transistor 1240 is cut off for the duration of each pulse and then conducts for the entire period separating succeeding pulses The, output volta@-e of transistor 1240, which appears across collector load resistor R1211, stands at -7.5 volts 10 when no uhguarded multiplexer pulses are received. Iiurin.- periods when unguarded multiplexer ptilses are being rece:.Ved, the output voltage rises to approximately +4.5 volts except for very short intervals once per frame when the voltage once more drops to -7.5 volts. i5 The output signal is applied to an integrator circuit comprising resistor R1212 and capacitor C1207. The output of this integrator circuit is connected to the emitter of monostable oscillator transistor 1250. The time constant of the integrator is so chosen that approximately 20 one second is required for the output to build up to a potential high enou.-h, to trigger the oscillator. In this way, mom I entary unguarded multiplexer pulses will not operate the emergency pulse circuit, but the prolonged existence of unguarded multii)lexer pulses will result in 25 the operation of the circuit. The resulting negative oiitput pulse from transistor 1250 is coupled through diode CD1211 to the base circuit of ring driver transistor 1220 w@hich functions to step the ring, as previously described. A manual push button PB is incorporated in the 30 emergency pulse generator circuit to serve as a means for advancing the allotter one step at a time for test purposes. If the button is held down, the allotter will step continuously at a slow rate. Resistor R1213 and capacitor C1207 comprise the integrator circuit in this 35 condition. The emergency pulse generator circuit will also respond as a result of allotter ring failure. If the ring, fails to step, the allotter will not allot a new finder. If a line goes off hook, no finders are capable of seizing that line, 40 and the multiplexer pulses remain unguardedi thiis causing the operation of the emergency pulse generator. The emergency pulse generator will also be energized in the event that all finders are busy. The allotter will step continuously, trying to find an idle finder, under con- 45 trol of the "and" gates associated with the ring stages. Since the multiplexer pulses remain unguarded, the emergency service circuit will also be operated. As used in this circuit, transistors 1200A, 1200B, 1200C, 1230, 1250, and 1220 may be type GIIA, tran- 50 sistors 1210A, 1210B, and 1210C may be type TI201, and transistor 1240 may be type CK722. While the allotter has been disclosed as controlling finders in a bi-path system, its application is not limited thereto. Allotter 19 could be used in an all multiplex 55 system such as that shown in Morris and Trousdale application Ser. No. 134,974, which application is assigned to the same assignee as the present invention. LINK EQUIPMENT 60 Line finder 17A This circuit is shown in Figures 19 and 20 of the drawings. The circuit comprises a control section-and A register section. The control section --omprises in gate amplifier transistor 1900, cut-through start transistor 1910, 65 cut-through hold transistor 1920, release delay transistor 1930, cut-through output transistor 1940 allotter start transistor 1950A and arotter start 1 tra'nsistor 1950B. The pulse generating or register section, which functions to generate a pulse in the time position bf the calling line, 70 comprises the units register pulser transistor 1960, the units register circuit, tens register pulser transistor 2000, the tens register circuit, and a two stage amplifier comprising transistors 2040 and 2050. As will be explained more fully hereinafter, the register circuits of the finder 75, are continuously operated while the finder is idle and are

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L6: Entry 3 of 8 File: USPT Apr 27, 1993

DOCUMENT-IDENTIFIER: US 5206948 A
TITLE: Bus monitor with means for selectively capturing trigger conditions

Abstract Text (1):
A monitoring means for selectively detecting and recording signals representing at selected points within a system, includes trigger generation logic responsive to selected bus signals for generating trigger signals representing the occurrence of selected conditions, and a recording memory for recording the conditions thereupon, a trigger selection logic for selecting trigger outputs corresponding to the trigger signals. The trigger selection logic includes a trigger enabling memory for storing selectable trigger enabling codes, wherein each enabling code corresponds to a trigger signal, and trigger output logic responsive to the trigger enabling codes and to the trigger signals for providing trigger outputs. The trigger enabling codes include bus enabling codes representing selected conditions on a bus of the system, trigger sequence enabling codes corresponding to sequential combinations of trigger signals and external trigger enabling codes corresponding to triggers external to the system. The enabling codes may select trigger signals to be used in logical AND or OR functions in generating a trigger output or in substitution for a bus trigger signal.

Detailed Description Text (28):
The primary elements comprising Trigger Control 38 are shown in the lower right portion of FIG. 2 and include Trigger Enable Register (TRIGENR) 90, Trigger Memory (TRIGMEM) 92, Illegal/Error Condition Detector (ILGL/ER) 94, Trigger Detector Logic (TRIGDET) 96, Trigger Registers (TRIGREG) 98 and Time Stamp Counter (TSC) 100. As will be described below, the outputs from TRIGMEM 92, ELGL/ER 94 and the inputs from EXTTRG 42 are trigger signals representing the occurrence of conditions being monitored while TRIGENR 90 stores information, in the form of trigger enabling codes, determining what particular monitored conditions will result in a sampling trigger while. TRIGDET 96 and TRIGREG 98 compare the triggers representing the occurrence of conditions being monitored with the present and previous trigger condition inputs from TRIGENR 90 and generate a trigger output, TRIGS, when a set of monitored conditions match the criteria stored in TRIGENR 90.

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L6: Entry 3 of 8 File: USPT Apr 27, 1993

US-PAT-NO: 5206948
DOCUMENT-IDENTIFIER: US 5206948 A

TITLE: Bus monitor with means for selectively capturing trigger conditions

DATE-ISSUED: April 27, 1993

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
De Angelis; Douglas J.	Woburn	MA		
Maddox; Henry W. J.	Franklin	MA		
Peters; Arthur	Sudbury	MA		
Rathbun; Donald J.	Methuen	MA		
Saltmarsh; William L.	Brockton	MA		

ASSIGNEE-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY	TYPE CODE
Bull HN Information Systems Inc.	Billerica	MA			02

APPL-NO: 07/ 455666 [PALM]
DATE FILED: December 22, 1989

INT-CL: [05] G06F 11/34

US-CL-ISSUED: 395/575; 371/19
US-CL-CURRENT: 714/45

FIELD-OF-SEARCH: 371/19.1, 371/15.1, 371/16.1, 364/2MSFile, 364/9MSFile

PRIOR-ART-DISCLOSED:

U.S. PATENT DOCUMENTS

Search Selected Search ALL Clear

	PAT-NO	ISSUE-DATE	PATENTEE-NAME	US-CL
☐	4100532	July 1978	Farnback	340/146.3MA
☐	4429368	January 1984	Kurii	371/19
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☐	4636940	January 1987	Goodwin, Jr.	371/19
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☐	4713813	December 1987	Sugimori et al.	371/15
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☐	4953167	August 1990	Byers et al.	371/16.5
☐	4982387	January 1991	Trent	368/117

ART-UNIT: 233

PRIMARY-EXAMINER: Beausoliel, Jr.; Robert W.

ASSISTANT-EXAMINER: Chung; Phung M.

ATTY-AGENT-FIRM: Clapp; Gary D. Solakian; John S.

ABSTRACT:

A monitoring means for selectively detecting and recording signals representing at selected points within a system, includes trigger generation logic responsive to selected bus signals for generating trigger signals representing the occurrence of selected conditions, and a recording memory for recording the conditions thereupon, a trigger selection logic for selecting trigger outputs corresponding to the trigger signals. The trigger selection logic includes a trigger enabling memory for storing selectable trigger enabling codes, wherein each enabling code corresponds to a trigger signal, and trigger output logic responsive to the trigger enabling codes and to the trigger signals for providing trigger outputs. The trigger enabling codes include bus enabling codes representing selected conditions on a bus of the system, trigger sequence enabling codes corresponding to sequential combinations of trigger signals and external trigger enabling codes corresponding to triggers external to the system. The enabling codes may select trigger signals to be used in logical AND or OR functions in generating a trigger output or in substitution for a bus trigger signal.

32 Claims, 3 Drawing figures

US005226153A

United States Patent [19]

DeAngelis et al.

[11] Patent Number: 5,226,153

[45] Date of Patent: Jul. 6, 1993

[54] **BUS MONITOR WITH TIME STAMP MEANS FOR INDEPENDENTLY CAPTURING AND CORRELATING EVENTS**

[75] Inventors: Douglas J. DeAngelis, Woburn; Henry W. J. Maddox, Franklin; Arthur Peters, Sudbury; Donald J. Rathbun, Methuen, all of Mass.

[73] Assignee: Bull HN Information Systems Inc., Billerica, Mass.

[21] Appl. No.: 944,793

[22] Filed: Sep. 14, 1992

Related U.S. Application Data

[63] Continuation of Ser. No. 455,668, Dec. 22, 1989, abandoned.

[51] Int. Cl.[5] G06F 11/30; G06F 11/34

[52] U.S. Cl. 395/575; 364/550; 364/DIG. 1; 364/264; 364/921.8; 364/949.3; 364/242.4; 340/825.06

[58] Field of Search 395/575; 371/29.1, 68.3; 364/550; 340/825.06

[56] **References Cited**

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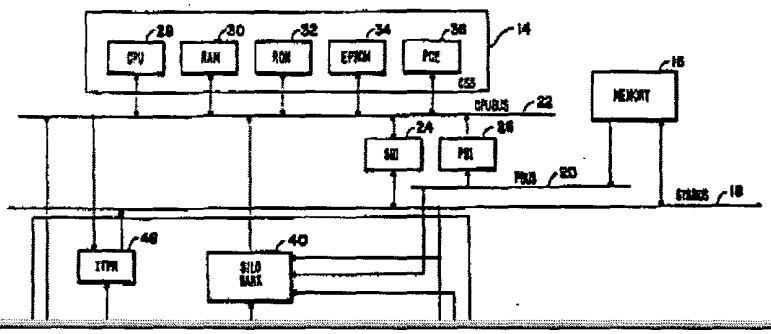
Primary Examiner—Eddie P. Chan
Attorney, Agent, or Firm—Gary D. Clapp; John S. Solakian

[57] **ABSTRACT**

A monitor for selectively detecting and recording conditions at selected points within a system during operation includes trigger logic connected from first selected points and responsive to selected conditions occurring at each of the first points for generating corresponding trigger outputs representing the occurrence of the selected conditions and a silo bank memory having a sub-silo for each second point. Each sub-silo has a first sub-silo segment with data inputs connected from the corresponding second point for recording data from the second point and a second sub-silo segment with data inputs connected from a time stamp generator. Silo write control logic is responsive to the trigger outputs to write the data representing the conditions present at each second point and the time stamp output of the time stamp generator into the corresponding sub-silo segments of the silo bank upon occurrence of a corresponding trigger output so that each condition recorded in the silo bank memory as the result of a trigger output has associated with it the time stamp count representing the relative time of occurrence of the trigger output.

11 Claims, 4 Drawing Sheets



US005210862A

United States Patent [19]

DeAngelis et al.

[11] Patent Number: 5,210,862

[45] Date of Patent: May 11, 1993

[54] **BUS MONITOR WITH SELECTIVE CAPTURE OF INDEPENDENTLY OCCURING EVENTS FROM MULTIPLE SOURCES**

[75] Inventors: Douglas J. DeAngelis, Woburn; Henry W. J. Maddox, Franklin; Arthur Peters, Sudbury; Donald J. Rathbun, Methuen; William L. Saltmarsh, Brockton, all of Mass.

[73] Assignee: Bull HN Information Systems Inc., Billerica, Mass.

[21] Appl. No.: 455,667

[22] Filed: Dec. 22, 1989

[51] Int. Cl.[5] G06F 11/34

[52] U.S. Cl. 395/575; 364/267; 364/267.2; 364/DIG. 1

[58] Field of Search 364/200, 900; 371/15.1, 371/16.1, 19

[56] References Cited

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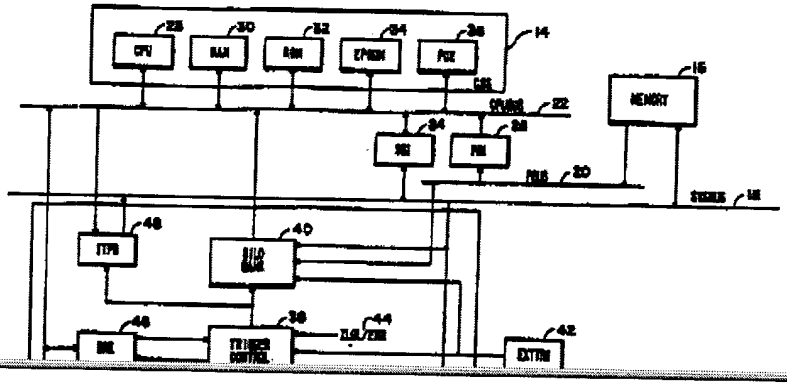
Primary Examiner—Robert W. Beausoliel
Attorney, Agent, or Firm—Gary D. Clapp; John S. Solakian

[57] ABSTRACT

A monitor device for selectively detecting and recording conditions at selected points within a system during operation, including a trigger enable memory for storing selectable trigger enabling codes wherein each code corresponds to a trigger signal representing the occurrence of a corresponding condition to be detected, a trigger generation device connected from first selected points and responsive to selected conditions thereupon for generating the trigger signals representing the occurrence of selected conditions, a trigger output device responsive to the enabling codes and the trigger signals for providing trigger outputs upon the occurrence of a trigger signal corresponding to a selected trigger enabling code, and a silo bank memory connected from second selected points and responsive to the trigger outputs for recording conditions present at the second points.

20 Claims, 5 Drawing Sheets



US005206948A

United States Patent [19]

De Angelis et al.

[11] Patent Number: 5,206,948

[45] Date of Patent: Apr. 27, 1993

[54] **BUS MONITOR WITH MEANS FOR SELECTIVELY CAPTURING TRIGGER CONDITIONS**

[75] Inventors: Douglas J. De Angelis, Woburn; Henry W. J. Maddox, Franklin; Arthur Peters, Sudbury; Donald J. Rathbun, Methuen; William L. Saltmarsh, Brockton, all of Mass.

[73] Assignee: Bull HN Information Systems Inc., Billerica, Mass.

[21] Appl. No.: 455,666

[22] Filed: Dec. 22, 1989

[51] Int. Cl.[5] G06F 11/34

[52] U.S. Cl. 395/575; 371/19

[58] Field of Search ..... 371/19.1, 15.1, 16.1; 364/200 MS File, 900 MS File

[56] References Cited

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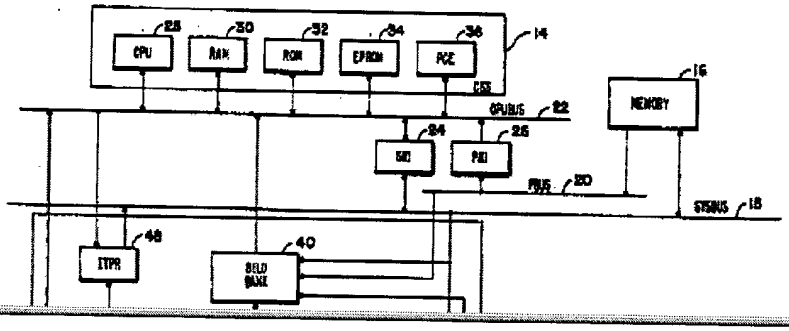
Primary Examiner—Robert W. Beausoliel, Jr.
Assistant Examiner—Phung M. Chung
Attorney, Agent, or Firm—Gary D. Clapp; John S. Solakian

[57] **ABSTRACT**

A monitoring means for selectively detecting and recording signals representing at selected points within a system, includes trigger generation logic responsive to selected bus signals for generating trigger signals representing the occurrence of selected conditions, and a recording memory for recording the conditions thereupon, a trigger selection logic for selecting trigger outputs corresponding to the trigger signals. The trigger selection logic includes a trigger enabling memory for storing selectable trigger enabling codes, wherein each enabling code corresponds to a trigger signal, and trigger output logic responsive to the trigger enabling codes and to the trigger signals for providing trigger outputs. The trigger enabling codes include bus enabling codes representing selected conditions on a bus of the system, trigger sequence enabling codes corresponding to sequential combinations of trigger signals and external trigger enabling codes corresponding to triggers external to the system. The enabling codes may select trigger signals to be used in logical AND or OR functions in generating a trigger output or in substitution for a bus trigger signal.

32 Claims, 3 Drawing Sheets



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L3: Entry 1 of 19 File: USPT Mar 16, 2004

DOCUMENT-IDENTIFIER: US 6707474 B1
TITLE: System and method for manipulating relationships among signals and buses of a signal measurement system on a graphical user interface

Brief Summary Text (9):
The trigger condition may be specified using occurrences such as shift in a signal value from low to high (rising edge) or a shift from high to low (falling edge). Also, a trigger condition may be specified with reference to a signal state, such as a "logic high" state or a "logic low" state. These occurrences or states may be referred to as "events" for purposes of specifying a trigger condition. Alternatively, a trigger condition may be specified by requiring that a number of events occur simultaneously, or in a specified time sequence. Any of the logic signals received by the logic analyzer may be used to specify a trigger condition. The term "bus" conventionally is used to refer to a group of channels that are conceptually grouped together even though they need not be physically grouped together. Thus, for example, a bus may be defined as including channels A, B, and C to assist a designer in comparing and analyzing the signals present on those channels. To this end, the signals conceptually grouped together in the bus often are displayed together on a display device where they may be observed or measured by the designer. These signals may be displayed as waveforms. Also, the values of the signals in the bus at a particular instant, collectively referred to as the "bus value" at that time, may be displayed. For example, the logic analyzer may determine that the value of the signal A at a particular time is the binary value "0," the value of the signal B is "1" at that time, and the value of the signal C is "0" at that time. The bus consisting of those signals may then be said to have the binary value "010," which may also be expressed as a hexadecimal value, or a value in any other base.

Detailed Description Text (19):
As noted, signal processor 140 samples and digitizes logic signals from the device under test, compares the resulting sampled data to user-selected trigger conditions, and, when the sampled data match the trigger conditions and satisfy user-selected trigger position requirements, stores user-selected portions of the sampled data in a display memory. Device under test 135 of the illustrated embodiment may be any of a variety of known or existing devices that produce, or have operations that may be assessed by measuring, logic signals or other types of analog or digital waveforms. For example, device under test 135 may be a microprocessor, random access memory, another type of chip or chip set, a data bus or address bus, or another input-output bus or other communication channel. For illustrative purposes, it is assumed that device under test 135 has a number of measurement points at which any conventional probe device may be connected to measure logic states represented by analog voltages. The illustrative analog voltages measured in this manner are hereafter referred to as logic signals 132. For convenience, logic signals 132 are shown in the Figures as a single data line, but it will be understood that each of logic signals 132 may be carried on a single wire or other communication channel (not shown) so that multiple wires or channels carry logic signals 132 from device under test 130 to signal processor 140. Alternatively, in other embodiments, some or all of logic signals 132 may be multiplexed so as to be carried over one communication channel in accordance with known techniques.

Detailed Description Text (148):
A further drawing rule is illustrated by FIGS. 15N and O. In FIG. 15N, user 101 has drawn rising edge 15100 on constant-time line 15101. User 101 has not yet entered a trigger-condition element for a second signal, as indicated by the dashed waveform 15102. In FIG. 15O, it is shown that user 101 has now drawn rising edge 15104 for the second signal on constant-time line 15103 that follows constant-time line 15101. It is illustratively assumed, however, that user 101 has not drawn a trigger-condition element for the first signal on constant-time line 15103. Display coordinator 630 therefore applies a drawing rule in accordance with the illustrated embodiment so that rising edge 15100 is extended to line 15103. That is, the high logic state resulting from rising edge 15100 is extended to line 15103. More generally, the rule is that when user 101 specifies a trigger-condition element for a first signal on a first constant-time line but not on a subsequent constant-time line, and user 101 specifies a trigger-condition element for a second signal or for a bus on that subsequent constant-time line, display coordinator 630 extends the trigger-condition element for the first signal from the first constant-time line to the subsequent constant-time line. User 101 may override this rule by drawing a trigger-condition element for the first signal on line 15103. This rule for extending signals may be compared with the rule in accordance with the illustrated embodiment for extending buses, as described above with respect to FIG. 15J. As noted, buses are extended under similar circumstances by adding "don't care" conditions rather than by extending the existing trigger condition. The difference is a matter of anticipating the likely intentions of user 101 under typical operating conditions, and the rules may thus be otherwise in alternative embodiments.

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L3: Entry 1 of 19 File: USPT Mar 16, 2004

US-PAT-NO: 6707474
DOCUMENT-IDENTIFIER: US 6707474 B1

TITLE: System and method for manipulating relationships among signals and buses of a signal measurement system on a graphical user interface

DATE-ISSUED: March 16, 2004

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Beck; Douglas James	Colorado Springs	CO		
Upham; Michael A.	Colorado Springs	CO		
Brown; Cheryl	Colorado Springs	CO		

ASSIGNEE-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY	TYPE CODE
Agilent Technologies, Inc.	Palo Alto	CA			02

APPL-NO: 09/ 430108 [PALM]
DATE FILED: October 29, 1999

PARENT-CASE:
RELATED APPLICATIONS The following applications are related to the present application: U.S. patent application Ser. No. 09/430,197 entitled "System and Method for Specifying Trigger Conditions of a Signal Measurement Using Hierarchical Structures On A Graphical User Interface," assigned to the assignee of the present invention and filed concurrently herewith; U.S. patent application Ser. No. 09/430,203 entitled "System and Method for Specifying Trigger Conditions of a Signal Measurement System Using Graphical Elements on a Graphical User Interface," assigned to the assignee of the present invention and filed concurrently herewith; U.S. patent application Ser. No. 09/432,840 entitled "System and Method for Defining and Grouping Signals and Buses of a Signal Measurement System Using Selection Lists on a Graphical User Interface," assigned to the assignee of the present invention and filed concurrently herewith. The specification of the foregoing related applications are hereby incorporated herein by reference.

INT-CL: [07] G06 F 3/14

US-CL-ISSUED: 345/771; 345/773, 345/735, 345/739, 345/769, 345/810, 702/66, 702/67, 702/68
US-CL-CURRENT: 345/771; 345/735, 345/739, 345/769, 345/773, 345/810, 702/66, 702/67, 702/68

FIELD-OF-SEARCH: 345/771, 345/773, 345/965, 345/835, 345/839, 345/769, 345/440.1, 345/810, 702/57, 702/66, 702/67, 702/68, 702/117

PRIOR-ART-DISCLOSED:

U.S. PATENT DOCUMENTS

Search Selected | Search ALL | Clear

	PAT-NO	ISSUE-DATE	PATENTEE-NAME	US-CL
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☐	6327544	December 2001	Samuels	345/501

ART-UNIT: 2174

PRIMARY-EXAMINER: Sax; Steven

ASSISTANT-EXAMINER: Nguyen; Thomas T.

ABSTRACT:

A system is disclosed for manipulating buses and signals on a display window of a graphical user interface of a logic analyzer. Each signal is associated on the display with representations of its sampled data, which may be in the form of lists or of waveforms. The system enables a user to graphically associate the buses and signals. Also, the buses and signals may be visually associated on the display window with user-specified trigger-conditions. The User may graphically associate the signals into buses by selecting the signals then grouping them by selecting a group command. Responsive to this grouping, the system may generate a bus representing the grouped signals. The bus may be graphically associated with the grouped signal-name elements, such as, for example, by a hierarchical structure. The system, responsive to the grouping by the user of the signals into buses, generates bus-data elements representing signal data associated with the grouped signals. The system may visually associate the bus with the bus-data element, either by horizontal or vertical alignment.

39 Claims, 53 Drawing figures

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L3: Entry 1 of 19 File: USPT Mar 16, 2004

US-PAT-NO: 6707474
DOCUMENT-IDENTIFIER: US 6707474 B1

TITLE: System and method for manipulating relationships among signals and buses of a signal measurement system on a graphical user interface

DATE-ISSUED: March 16, 2004

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Beck; Douglas James	Colorado Springs	CO		
Upham; Michael A.	Colorado Springs	CO		
Brown; Cheryl	Colorado Springs	CO		

ASSIGNEE-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY	TYPE CODE
Agilent Technologies, Inc.	Palo Alto	CA			02

APPL-NO: 09/ 430108 [PALM]
DATE FILED: October 29, 1999

PARENT-CASE:
RELATED APPLICATIONS The following applications are related to the present application: U.S. patent application Ser. No. 09/430,197 entitled "System and Method for Specifying Trigger Conditions of a Signal Measurement Using Hierarchical Structures On A Graphical User Interface," assigned to the assignee of the present invention and filed concurrently herewith; U.S. patent application Ser. No. 09/430,203 entitled "System and Method for Specifying Trigger Conditions of a Signal Measurement System Using Graphical Elements on a Graphical User Interface," assigned to the assignee of the present invention and filed concurrently herewith; U.S. patent application Ser. No. 09/432,840 entitled "System and Method for Defining and Grouping Signals and Buses of a Signal Measurement System Using Selection Lists on a Graphical User Interface," assigned to the assignee of the present invention and filed concurrently herewith. The specification of the foregoing related applications are hereby incorporated herein by reference.

INT-CL: [07] G06 F 3/14

US-CL-ISSUED: 345/771; 345/773, 345/735, 345/739, 345/769, 345/810, 702/66, 702/67, 702/68
US-CL-CURRENT: 345/771; 345/735, 345/739, 345/769, 345/773, 345/810, 702/66, 702/67, 702/68

FIELD-OF-SEARCH: 345/771, 345/773, 345/965, 345/835, 345/839, 345/769, 345/440.1, 345/810, 702/57, 702/66, 702/67, 702/68, 702/117

PRIOR-ART-DISCLOSED:

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U.S. PATENT DOCUMENTS

Search Selected | Search ALL | Clear

	PAT-NO	ISSUE-DATE	PATENTEE-NAME	US-CL
☐	4455624	June 1984	Haag et al.	345/744
☐	4951190	August 1990	Lane et al.	364/188
☐	5371851	December 1994	Pieper et al.	395/507
☐	5481741	January 1996	McKaskle et al.	395/800
☐	5884306	March 1999	Bliss et al.	707/7
☐	5953009	September 1999	Alexander	345/348
☐	5977971	November 1999	Guzak et al.	345/853
☐	6054984	April 2000	Alexander	345/339
☐	6327544	December 2001	Samuels	345/501

ART-UNIT: 2174

PRIMARY-EXAMINER: Sax; Steven

ASSISTANT-EXAMINER: Nguyen; Thomas T.

ABSTRACT:

A system is disclosed for manipulating buses and signals on a display window of a graphical user interface of a logic analyzer. Each signal is associated on the display with representations of its sampled data, which may be in the form of lists or of waveforms. The system enables a user to graphically associate the buses and signals. Also, the buses and signals may be visually associated on the display window with user-specified trigger-conditions. The User may graphically associate the signals into buses by selecting the signals then grouping them by selecting a group command. Responsive to this grouping, the system may generate a bus representing the grouped signals. The bus may be graphically associated with the grouped signal-name elements, such as, for example, by a hierarchical structure. The system, responsive to the grouping by the user of the signals into buses, generates bus-data elements representing signal data associated with the grouped signals. The system may visually associate the bus with the bus-data element, either by horizontal or vertical alignment.

39 Claims, 53 Drawing figures

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L3: Entry 6 of 19 File: USPT May 27, 2003

DOCUMENT-IDENTIFIER: US 6570592 B1
TITLE: System and method for specifying trigger conditions of a signal measurement system using graphical elements on a graphical user interface

Brief Summary Text (9):
The trigger condition may be specified using occurrences such as shift in a signal value from low to high (rising edge) or a shift from high to low (falling edge). Also, a trigger condition may be specified with reference to a signal state, such as a "logic high" state or a "logic low" state. These occurrences or states may be referred to as "events" for purposes of specifying a trigger condition. Alternatively, a trigger condition may be specified by requiring that a number of events occur simultaneously, or in a specified time sequence. Any of the logic signals received by the logic analyzer may be used to specify a trigger condition. The term "bus" conventionally is used to refer to a group of channels that are conceptually grouped together even though they need not be physically grouped together. Thus, for example, a bus may be defined as including channels A, B, and C to assist a designer in comparing and analyzing the signals present on those channels. To this end, the signals conceptually grouped together in the bus often are displayed together on a display device where they may be observed or measured by the designer. These signals may be displayed as waveforms. Also, the values of the signals in the bus at a particular instant, collectively referred to as the "bus value" at that time, may be displayed. For example, the logic analyzer may determine that the value of the signal A at a particular time is the binary value "0," the value of the signal B is "1" at that time, and the value of the signal C is "0" at that time. The bus consisting of those signals may then be said to have the binary value "010," which may also be expressed as a hexadecimal value, or a value in any other base.

Detailed Description Text (19):
As noted, signal processor 140 samples and digitizes logic signals from the device under test, compares the resulting sampled data to user-selected trigger conditions, and, when the sampled data match the trigger conditions and satisfy user-selected trigger position requirements, stores user-selected portions of the sampled data in a display memory. Device under test 135 of the illustrated embodiment may be any of a variety of known or existing devices that produce, or have operations that may be assessed by measuring, logic signals or other types of analog or digital waveforms. For example, device under test 135 may be a microprocessor, random access memory, another type of chip or chip set, a data bus or address bus, or another input-output bus or other communication channel. For illustrative purposes, it is assumed that device under test 135 has a number of measurement points at which any conventional probe device may be connected to measure logic states represented by analog voltages. The illustrative analog voltages measured in this manner are hereafter referred to as logic signals 132. For convenience, logic signals 132 are shown in the Figures as a single data line, but it will be understood that each of logic signals 132 may be carried on a single wire or other communication channel (not shown) so that multiple wires or channels carry logic signals 132 from device under test 130 to signal processor 140. Alternatively, in other embodiments, some or all of logic signals 132 may be multiplexed so as to be carried over one communication channel in accordance with known techniques.

Detailed Description Text (143):
A further drawing rule is illustrated by FIGS. 15N and O. In FIG. 15N, user 101 has drawn rising edge 15100 on constant-time line 15101. User 101 has not yet entered a trigger-condition element for a second signal, as indicated by the dashed waveform 15102. In FIG. 15O, it is shown that user 101 has now drawn rising edge 15104 for the second signal on constant-time line 15103 that follows constant-time line 15101. It is illustratively assumed, however, that user 101 has not drawn a trigger-condition element for the first signal on constant-time line 15103. Display coordinator 630 therefore applies a drawing rule in accordance with the illustrated embodiment so that rising edge 15100 is extended to line 15103. That is, the high logic state resulting from rising edge 15100 is extended to line 15103. More generally, the rule is that when user 101 specifies a trigger-condition element for a first signal on a first constant-time line but not on a subsequent constant-time line, and user 101 specifies a trigger-condition element for a second signal or for a bus on that subsequent constant-time line, display coordinator 630 extends the trigger-condition element for the first signal from the first constant-time line to the subsequent constant-time line. User 101 may override this rule by drawing a trigger-condition element for the first signal on line 15103. This rule for extending signals may be compared with the rule in accordance with the illustrated embodiment for extending buses, as described above with respect to FIG. 15J. As noted, buses are extended under similar circumstances by adding "don't care" conditions rather than by extending the existing trigger condition. The difference is a matter of anticipating the likely intentions of user 101 under typical operating conditions, and the rules may thus be otherwise in alternative embodiments.

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L3: Entry 6 of 19 File: USPT May 27, 2003

US-PAT-NO: 6570592
DOCUMENT-IDENTIFIER: US 6570592 B1

TITLE: System and method for specifying trigger conditions of a signal measurement system using graphical elements on a graphical user interface

DATE-ISSUED: May 27, 2003

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Sajdak; Gregory J	Coloraado Springs	CO		
Beck; Douglas James	Colorado Springs	CO		
Upham; Michael A.	Colorado Springs	CO		

ASSIGNEE-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY	TYPE CODE
Agilent Technologies, Inc.	Palo Alto	CA			02

APPL-NO: 09/ 430203 [PALM]
DATE FILED: October 29, 1999

PARENT-CASE:
RELATED APPLICATIONS The following applications are related to the present application: U.S. patent application Ser. No. 09/430,108 entitled "System and Method for Manipulating Relationships Among Signals and Buses of a Signal Measurement System on a Graphical User Interface," assigned to the assignee of the present invention and filed concurrently herewith; U.S. patent application Ser. No. 09/430,197 entitled, "System and Method for Specifying Trigger Conditions of a Signal Mesurement Using Hierachical Structures On A Graphical User Interface," assigned to the asignee of the present invention and filed concurently herewith; U.S. patent application Ser. No. 09/432,840 entitled "System and Method for Defining and Grouping Signals and Buses of a Measurement System Using Selection Lists on a Graphical User Interface," assigned to the assignee of the present invention and filed concurrently herewith. The specification of the foregoing related applications are hereby incorporated herein by reference.

INT-CL: [07] G06 F 3/14

US-CL-ISSUED: 345/769; 345/835, 345/771, 345/440.1, 345/839, 345/773
US-CL-CURRENT: 345/769; 345/440.1, 345/771, 345/773, 345/835, 345/839

FIELD-OF-SEARCH: 345/440.1, 345/771, 345/773, 345/965, 345/835, 345/839, 345/769, 345/94, 702/57, 702/66, 702/67, 702/68, 702/117

PRIOR-ART-DISCLOSED:

U.S. PATENT DOCUMENTS

Search Selected | Search ALL | Clear

	PAT-NO	ISSUE-DATE	PATENTEE-NAME	US-CL
☐	5371851	December 1994	Pieper et al.	395/507
☐	5892948	April 1999	Aoki et al.	395/701
☐	5953009	September 1999	Alexander	345/348
☐	6259993	July 2001	Hori	702/30
☐	6327544	December 2001	Samuels	702/70

ART-UNIT: 2174

PRIMARY-EXAMINER: Kincaid; Kristine

ASSISTANT-EXAMINER: Nguyen; Thomas T.

ABSTRACT:

A system is disclosed for enabling a user to specify one or more trigger conditions by graphically creating a pictorial representation of the trigger conditions. The pictorial representation is presented on a display window of a graphical user interface of a logic analyzer and is accomplished using trigger-condition icons. Each icon represents a trigger condition of a signal or bus. The user specifies the trigger conditions by positioning the trigger-condition icons on the display window. The user does this by selecting, dragging, and dropping the trigger-condition icons onto the display window. The display window may include one or more name elements, each associated with a signal or a bus. The user may specify the trigger condition of a first signal or bus by selecting a trigger-condition icon and positioning it at a first position on the display window in horizontal alignment with the name element of the first signal or bus. Responsive to this action, the system displays a first trigger-condition element at the first position. The user may select the trigger-condition icon from a group of icons consisting of rising-edge icon, falling-edge icon, either-edge icon, low-level icon, high-level icon, don't care icon, bus icon, positive pulse icon, and negative pulse icon. The display window may include one or more vertically aligned constant time lines. The first position may be located on a first constant-time line, and the user may select other position on other constant-time lines. The user may specify a time-limit between the first and second constant-time lines, and or between the second and third constant-time lines. This specification may be that the time-limit is an indefinite time period, or that it is less than or greater than a user-specified time period. The system includes a trigger specifier that determines a combined trigger condition for a first state corresponding to the first constant-time line based on the first and second trigger-condition elements and one or more boolean expressions. These expressions may be predetermined, or they may be user-specified.

29 Claims, 53 Drawing figures

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L3: Entry 6 of 19 File: USPT May 27, 2003

US-PAT-NO: 6570592
DOCUMENT-IDENTIFIER: US 6570592 B1

TITLE: System and method for specifying trigger conditions of a signal measurement system using graphical elements on a graphical user interface

DATE-ISSUED: May 27, 2003

INVENTOR-INFORMATION:

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Sajdak; Gregory J	Coloraado Springs	CO		
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Upham; Michael A.	Colorado Springs	CO		

ASSIGNEE-INFORMATION:

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US-CL-CURRENT: 345/769; 345/440.1, 345/771, 345/773, 345/835, 345/839

FIELD-OF-SEARCH: 345/440.1, 345/771, 345/773, 345/965, 345/835, 345/839, 345/769, 345/94, 702/57, 702/66, 702/67, 702/68, 702/117

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☐	6327544	December 2001	Samuels	702/70

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